# Shanghai Siproin Microelectronics Co.,Ltd.

# Three-phase power metering integrated circuits

# SSP1880

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# Contents

# 1.General Description

The SSP1880 is a highly accurate three-phase power measurement integrated circuit with technical specifications that meet the accuracy requirements specified in IEC62053.。

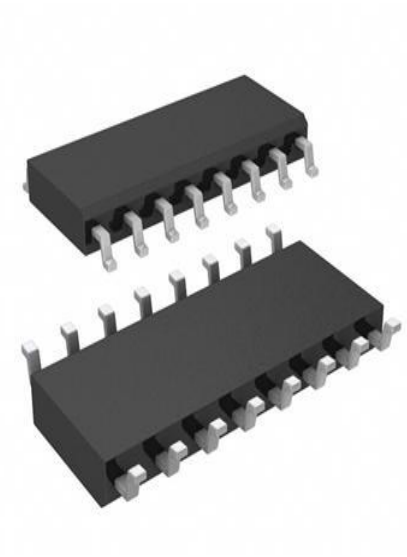
The SSP1880 uses analogue circuitry only for the ADC and reference source, and digital circuitry for all other signal processing (such as multiplication and filtering), which allows the SSP1880 to maintain extremely high accuracy and long-term stability under harsh environmental conditions.

The SSP1880 pins F1 and F2 output the average value of active power at a lower frequency and can be used to directly drive electromechanical meters or to interface with microcontrollers (MCUs). Pin CF outputs an instantaneous value of active power at a higher frequency for calibration or interfacing with an MCU.

The SSP1880 contains an internal monitoring circuit for the VDD power supply pin. The SSP1880 remains in reset until VDD rises to 4V. When VDD falls below 4V, the SSP1880 is also reset, at which point there are no outputs from F1, F2, or CF.

Internal phase matching circuitry enables the voltage and current channels to always be phase-matched, and internal no-load threshold characteristics ensure that the SSP1880 has no latency at no-load.

The SSP1880 is available in a 16-pin SOP package.



# 2.Features

- High accuracy, supporting the accuracy requirements of the 50Hz/60Hz IEC 62053 standard, with an error of less than 0.1 per cent over a dynamic range of 500:1;
- The active power average is output in frequency from SSP1880 pins F1 and F2;
- The active power instantaneous value is output from pin CF at a higher frequency and can be used for meter calibration;
- FI and F2 can directly drive electromechanical counters and two-phase stepper motors;
- The use of specialised analogue-to-digital converters (ADCs) and digital signal processing (DSPs) ensures a high degree of accuracy even under conditions of highly variable environment and time;
- Power monitoring circuitry is provided on-chip;
- Anti-submarine function (no-load threshold) is included in the chip;
- An on-chip reference voltage of 2.5V±8% (temperature coefficient typical 30ppm/°C) provides a reference for external circuits;
- A high stability oscillator with little sensitivity to temperature is included on the chip.
- +5V single-supply, low-power (15mW typical);
- Low-cost CMOS process.
- SOP16 package

# 3.Order Specification

| Product model | Package | Manner of packing | Min packing quantity |
|---|---|---|---|
| SSP1880 | SOP16 | Reels | 2500PCS |

## 4.Block Diagram

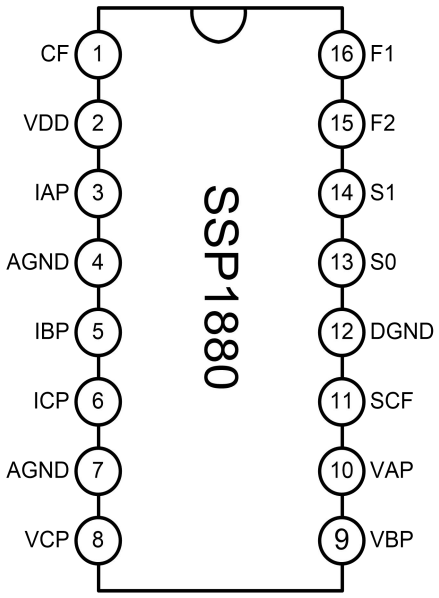



Figure (1) Pin Arrangement (SOP16 Package)

| Pin number | Symbol | Description |
|---|---|---|
| 1 | CF | Frequency calibration output pin. Its output frequency reflects the magnitude of instantaneous active power and is commonly used for instrument calibration, see IV table for description. |
| 2 | VDD | Power supply pin. This pin provides the power supply for the SSP1880, and the normal operating power supply voltage should be maintained at 5V ± 5%, and the pin should be decoupled using a 10μF capacitor in parallel with a 100nF ceramic dielectric capacitor. |
| 3，5，6 | IAP，IBP，ICP | Phase A, B, and C current channel inputs, respectively, with a maximum signal level of ±500 mV for normal operation. these three pins have internal ESD protection circuits, and these two pins can withstand ±6V overvoltage without causing permanent damage. |
| 8，9，10 | VCP，VBP，VAP | Respectively for the C-phase, B-phase, A-phase voltage channel inputs, the normal operation of the maximum signal level of ± 500 mV. these three pins have internal ESD protection circuitry, these two pins can withstand ± 6V over-voltage, without causing permanent damage. |
| 4，7 | AGND | This is the ground reference point for the SSP1880 analogue circuits and this pin is connected to the analogue ground of the printed circuit board. The analogue ground plane is the ground reference point for all analogue circuits, such as anti-alias filters, current and voltage sensors, and so on. For effective noise suppression, the analogue ground plane should be connected to the digital ground plane at only one point. |
| 11 | SCF | Check Frequency Selection. The logic input level of this pin determines the output frequency of the CF pin, see Table IV for how to select the calibration frequency. |

| | | |
|---|---|---|
| 13，14 | S1，S0 | The logic inputs to these two pins are used to select the digital/frequency conversion factor, which provides a great deal of flexibility in meter design, as detailed in the Selecting Frequency for Meter Applications section. |
| 15，16 | F2，F1 | The low frequency logic output pin, the output frequency responds to the amount of average active power. These two logic outputs can directly drive electromechanical meters or two-phase stepper motors, as detailed in the Transfer Functions section. |

## 5.Absolute Maximum Ratings

| Parameter name | Symbolic | Value | Unit |
|---|---|---|---|
| Chip Supply Voltage | VDD | -0.3～+7 | V |
| Analogue Signal Inputs | IAP, IBP, ICP, VAP, VBP, VCP to GND Voltage | -6～+6 | V |
| Reference Input Voltage | | -0.3～VDD+0.3 | V |
| Digital Input Voltage | | -0.3～VDD+0.3 | V |
| Digital Output Voltages | | -0.3～VDD+0.3 | V |
| Operating Temperature Range | T | -40～+85 | ℃ |
| Storage Temperature Range | Tstg | -40～+85 | ℃ |
| Junction Temperature | Tj | +150 | ℃ |
| SSOP24Package Power Dissipation | Pd | 450 | mW |
| Thermal Resistance | θJA | 112 | ℃/W |
| Vapour Phase Welding（60S） | | +215 | ℃ |
| Infrared Welding（15S） | | +220 | ℃ |

Note：Unless otherwise specified, TA = 25℃.

## 6.Electrical Characteristics

| **Measurement items** | Symbolic | **Measurement Conditions** | **Min** | **Typical** | **Max** | **Unit** |
|---|---|---|---|---|---|---|
| Chip Operating Voltage | VDD | | 4.75 | 5 | 5.25 | V |
| Chip Working Current | $I_{DD}$ | | 5 | 6.5 | 8 | mA |
| Measurement error of the current channel | | Channel 2 is full input (±500mV), +25℃, dynamic range 500:1 | | 0.1 | | % |
| Phase error between current and voltage channels | | Line frequency 45-65Hz, V1 overrun by 37°（PF=0.8 capacitive） | | ±0.1 | | % |
| | | Line frequency 45-65Hz,, V1 hysteresis 60° (PF = 0.5 inductive) | | ±0.1 | | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| AC power supply suppresses output frequency variations（CF） | | SCF=0，S1=S0=1，<br>IA=IB=IC=100mVrms，50Hz<br>VA=VB=VC=100mVrms，50Hz<br>VDD plus 200 mV rms, 100Hz ripple | | 0.2 | | % |
| DC power supply suppresses output frequency variations（CF） | | S1=1，S0=SCF=0<br>IA=IB=IC=100mV rms，50Hz<br>VA=VB=VC=100mVrms，50Hz<br>VDD =5V±250mV | | ±0.3 | | % |
| **Analogue Inputs** | | | | | | |
| Max Signal Level | | VA, VB, VC, IA, IB, IC voltage to GND | | | ±0.5 | V |
| DC Input Resistance | | CLKOSC=10MHz | 390 | | | kΩ |
| -3dB bandwidths | | CLKOSC/256，CLKOSC=10MHz | | 14 | | KHZ |
| ADC misalignment error | | | | | ±16 | mV |
| Gain error | | External Reference Source 2.5V，<br>IAP=IBP=ICP=500mV ，dc | | ±9 | | % |
| **On-chip Reference Source** | | | | | | |
| Reference Voltage Error | | Nominal Value 2.5V | | | ±200 | mV |
| Temperature Coefficient | | Nominal Value 2.5V | | 30 | | ppm/°C |
| Clock Input | | | | | | |
| Input Clock Frequency | | All indicator CLKOSCs are 10MHz | 8 | 10 | 12 | MHZ |
| **logical input**<br>SCF，S0，S1，AC/DC，RESET，G0 and G1 | | | | | | |
| Input High Level | $V_{INH}$ | VDD=5V±5% | 2.4 | | | |
| Input Low Level | $V_{INL}$ | VDD=5V±5% | | | 0.8 | |
| Input Current | | $V_{IN}$=0V~VDD | | 0.01 | ±3 | μA |
| Input capacitance | | | | | 10 | pF |
| **logical output**<br>F1，F2 | | | | | | |
| Output High Level | $V_{OH}$ | $I_{SOURCE}$=10mA，VDD=5V | 4.5 | | | V |
| Output Low Level | $V_{OL}$ | $I_{SINK}$=10mA，VDD=5V | | | 0.5 | V |
| CF，REVP | | | | | | |
| Output High Level | $V_{OH}$ | $I_{SOURCE}$=10mA，VDD=5V | 4 | | | V |
| Output Low Level | $V_{OL}$ | $I_{SINK}$=10mA，VDD=5V | | | 0.5 | V |

Noted：Unless otherwise specified, TA = 25°C.

All voltage values use the GND terminal potential as a reference point.

VDD= 5V±5%, GND=0V, using on-chip reference source, CLKOSC=10MHz.

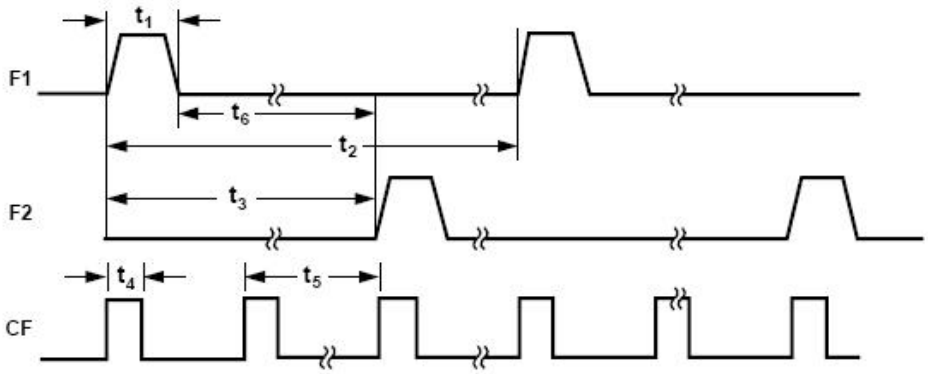
## 7.Timing Characteristics

（VDD= 5V±5%, GND=0V, using on-chip reference source, CLKOSC=10MHz, temperature range=-40 to +85℃）

| Parameters | tail mark A，B | unit | Test conditions and notes |
|---|---|---|---|
| $T_1$ Note(1) | 275 | ms | Bottom level pulse widths of F1 and F2 |
| $T_2$ | See table 1 below | s | Output pulse period, see transfer function section |
| $T_3$ | 1/2 $T_2$ | s | Time between F1 falling edge and F2 falling edge |
| $T_4$ Note(1, 2) | 96 | ms | High level pulse width of CF output |
| $T_5$ | See table 1 below | s | CF output pulse period, see transfer function section |
| $T_6$ | CLKOSC/4 | s | Min time between F1 and F2 pulses |

Note:(1) The pulse widths of F1, F2 and CF are not fixed at higher output frequencies.

(2) In the high frequency mode, the CF pulse width is always 18μs.




**Frequency output timing diagram**

## 8.Pulse Setting

| SCF | S1 | S0 | $F_{1\sim7}$ (Hz) | Max output frequency of CF(Hz) | Counter scale (C=Calibration constants) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1.27 | 160×F1，F2=81.87 | C/80 |
| 1 | 0 | 0 | 1.19 | 8×F1，F2=3.83 | C/4 |
| 0 | 0 | 1 | 5.09 | 160×F1，F2=327.46 | C/80 |
| 1 | 0 | 1 | 4.77 | 16×F1，F2=30.70 | C/8 |
| 0 | 1 | 0 | 19.07 | 16×F1，F2=122.81 | C/8 |
| 1 | 1 | 0 | 19.07 | 8×F1，F2=61.40 | C/4 |
| 0 | 1 | 1 | 76.29 | 8×F1，F2=245.61 | C/4 |
| 1 | 1 | 1 | 0.6 | 16×F1，F2=3.84 | C/8 |

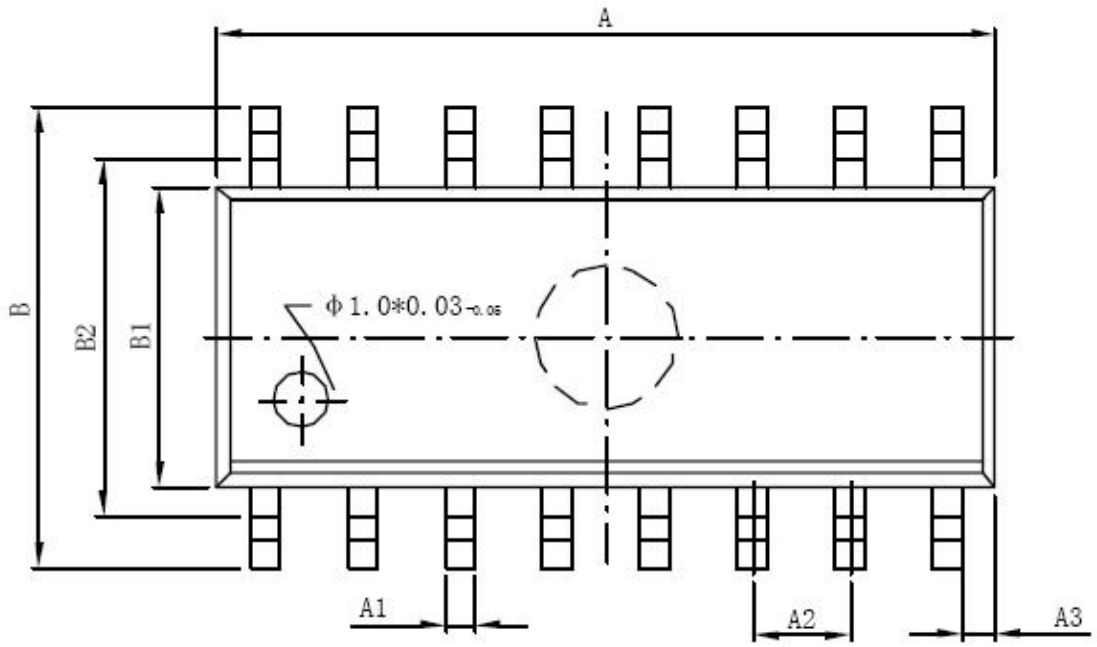
Table 1 Maximum output frequency of CF (AC signal)

## 9.Various common phenotype jumper settings and counter selection

| Max current（A） | Transformer ratio | Sampling Resistance（Ω） | Constant | Counter Ratio | SCF | | S0 | | S1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 1 | 0 | 1 | 0 | 1 |
| | | | | | J1 | J2 | J3 | J4 | J5 | J6 |
| 10<br>(Be applicable to<br>1.5~6.0<br>2.0~8.0<br>2.0~10.0) | 300:1 | 10 | 1600 | 200 | | ● | | ● | | ● |
| | | 10 | | 400 | | ● | ● | | ● | |
| | | 15* | 3200 | 400 | | ● | | ● | | ● |
| | | 15* | | 800 | | ● | ● | | ● | |
| 50<br>(Be applicable to<br>10~40<br>20~50) | 1000:1 | 5.1 | 160 | 20 | | ● | | ● | | ● |
| | | 5.1 | | 40 | | ● | ● | | ● | |
| | | 6 | 320 | 40 | | ● | | ● | | ● |
| | | 6 | | 80 | | ● | ● | | ● | |
| | | 9.1 | 400 | 50 | | ● | | ● | | ● |
| | | 9.1 | | 100 | | ● | ● | | ● | |
| 100<br>(Be applicable to<br>15~60<br>20~80<br>20~100) | 1000:1 | 3 | 160 | 20 | | ● | | ● | | ● |
| | | 3 | | 40 | | ● | ● | | ● | |
| | | 4.7 | 320 | 40 | | ● | | ● | | ● |
| | | 4.7 | | 80 | | ● | ● | | ● | |
| | 2000:1 | 6.2 | 160 | 20 | | ● | | ● | | ● |
| | | 6.2 | | 40 | | ● | ● | | ● | |
| | | 9.1 | 320 | 40 | | ● | | ● | | ● |
| | | 9.1 | | 80 | | ● | ● | | ● | |

Note：Depends on the maximum load resistance of the CT.

## 10.Outline Dimensions




| 尺寸 / 标注 | 最小（mm） | 最大（mm） | 尺寸 / 标注 | 最小（mm） | 最大（mm） |
|---|---|---|---|---|---|
| A | 9.9 | 10.10 | C4 | 0.2TYP | |
| A1 | 0.356 | 0.456 | D | 1.05TYP | |
| A2 | 1.27TYP | | D1 | 0.40 | 0.70 |
| A3 | 0.35TYP | | D2 | 0.22 | 0.42 |
| B | 5.84 | 6.24 | R1 | 0.15TYP | |
| B1 | 3.84 | 4.04 | R2 | 0.15TYP | |
| B2 | 5.0TYP | | θ1 | 8° TYP | |
| C | 1.35 | 1.55 | θ2 | 8° TYP | |
| C1 | 0.61 | 0.71 | θ3 | 4° TYP | |
| C2 | 0.54 | 0.64 | θ4 | 15° TYP | |
| C3 | 0.10 | 0.30 | | | |

## SPECIAL EXPLANATION

The final interpretation right of this specification belongs to our company

## DESCRIPTION OF VERSION CHANGE

Version：V1.01　　Author：Lifeng Liu　　Date：2021.9.14

Amendment record：

1.Instruction manu Al reformatted, some data checked