STT-MRAM Datasheet

PN256KNIA

Version:1.0

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Contents

1 Description

The PN256K is a 256K Bit/32K Byte IIC interface non-volatile memory. It adopts advanced PMTJ STT-MRAM technology to achieve read and write transmission of up to 400kHz, with excellent reliability and more than 20 years of data retention time..

Features :

PMTJ STT-MRAM technology

- STT technology
- 256K Bit/32K Byte

IIC interface

- Support standard mode (100kHz) and fast mode (400kHz)
- Schmitt trigger and noise suppression filter for SDA and SCL
- Fast write time (100ns min)

Operation voltage

- Typical Voltage Vcc 2.7V~3.6V

Operation Temperature range

- -40℃~85℃

Data protection

- Supports hardware write protection mode for full capacity, configurable via WP

Power consumption

- Sleep current 2μA (Typical value)
- Standby current 20μA (Typical value)
- Working current 400μA (typical write current @400KHz)

Reliability

- Write times 1E12
- Data retention >20years @85℃

Package

- SOP8

Order specification

Part No	Density	Operating voltage range	Package	Devices per bag/reel	Maximum Program/Erase Cycles	Operating temperature	Data retention
PN256KNIA	256K Bit/ 32K Byte	2.7V~3.6V	SOP8	2500pcs/reel	1E12	-40℃~85℃	≥20years @85℃

2 Pin Information

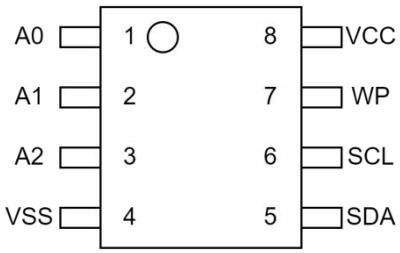


Figure 1: SOP8 Package Information (Top view)

Table1: Pin Description

No.	Symbol	Signal Type	Description
1	A0	Input	Address
2	A1	Input	Address
3	A2	Input	Connect to VSS or floating
4	VSS	Ground	Ground
5	SDA	Input/Output	Serial Input/Output
6	SCL	Input	Serial Clock
7	WP	Input	Write Protect
8	VCC	Power	Power Supply

Pin function description:

(1) A0, A1: Address pins are used to identify each device. Connect A0 and A1 to the VCC pin or VSS pin to define the device address. The chip will work only when the device address defined by A0 and A1 matches the device address word input by the SDA pin. The A0 and A1 pins have internal pull-down resistors. When they are in a floating state, they will be recognized as a low level by the chip. The same data bus supports up to 4 PN256K device connections

(2) A2: Must be connected to VSS or floating. It is not allowed to connect to VCC. The A2 pin has an internal pull-down resistor. When it is in a floating state, it will be recognized as a low level by the chip.

(3) VSS: Ground pin.

(4) SDA: Serial data input/output pin, which can be connected to multiple devices. This pin is an open-drain output and requires a pull-up resistor to connect to an external circuit.

(5) SCL: Clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge. This pin is an open-drain output and requires a pull-up resistor to connect to an external circuit.

(6) WP: Write protection pin. When connected to VCC, write operations are prohibited at all capacity. When connected to VSS, write operations are allowed at all capacity. The WP pin only affects write operations but not read operations. WP has a pull-down resistor inside. When it is floating, it is recognized as a low level by the chip.

(7) VCC: Power supply voltage pin.

3 Chip Function

PN256K supports IIC bus and runs as a slave device.

IIC bus defines the master and slave devices in the communication. The master device is responsible for initializing data transmission and generating clock signals for data synchronization. After being addressed by the master device, the slave device will respond to the addressing and exchange data with the master device.

Multiple devices can be mounted on an IIC bus, and each device has its corresponding device address. Data transmission between devices can only be transmitted by one device to the device with the corresponding address.

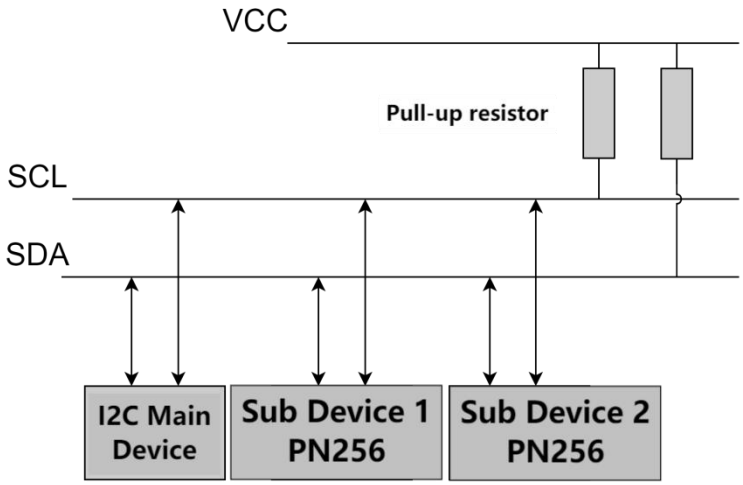


Figure 2: Interface System Configuration Example

3.1 IIC Protocol

Start Condition (S)

A change from high to low during the high period of SCL indicates a start condition. All commands should be preceded by a start condition. A start condition can terminate an ongoing

operation at any time.

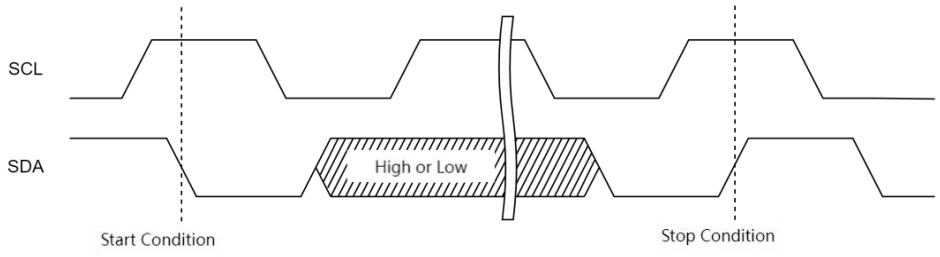


Figure 3: Start and Stop Conditions

Stop condition (P)

When SDA changes from low to high during SCL is high, it indicates a stop condition. The stop condition is used to end the current operation.

Data/address transmission

In the stop condition and start condition, the SDA level changes during SCL is high, while the data and address change during SCL is low and need to remain stable during SCL is high.

Acknowledgement (ACK) and non-acknowledgement (NACK)

In the IIC bus, serial data containing memory addresses or memory information is sent and received in groups of 8 bits. Each successful transmission or reception of a group of 8 bits of data means receiving or sending an acknowledgment signal. After each 8-bit data is sent, the sender temporarily enters a high impedance state at the 9th clock cycle to allow the reception and detection of the acknowledgment signal. In the high impedance release period, if the receiver pulls SDA down to a low level, a response signal ACK is given, indicating that the previous 8-bit data has been successfully received. If the receiver pulls SDA up to a high level, a non-acknowledgement signal NACK is given, indicating that the previous 8-bit data has failed to be received.

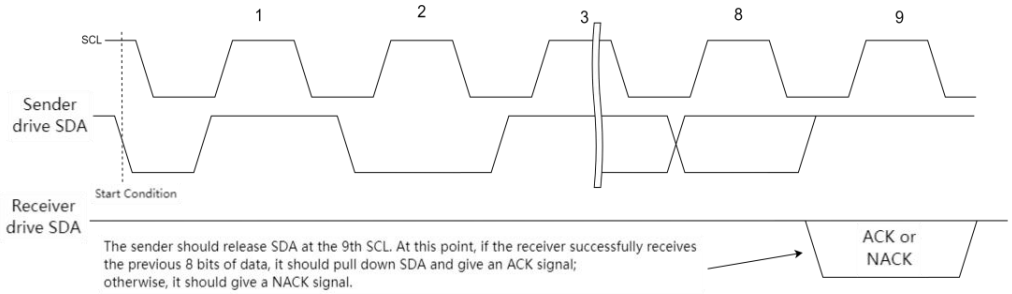


Figure4：Response timing diagram

3.2 Device address

After the start condition, input the 8-bit device address word, as shown in the figure below, where bit7-4 is the device type code, this chip is 1010, bit3-1 is the device address code, used to distinguish different devices mounted on the bus, bit0 is the read/write code (R/W), R/W=1 indicates a read operation, and R/W=0 indicates a write operation.

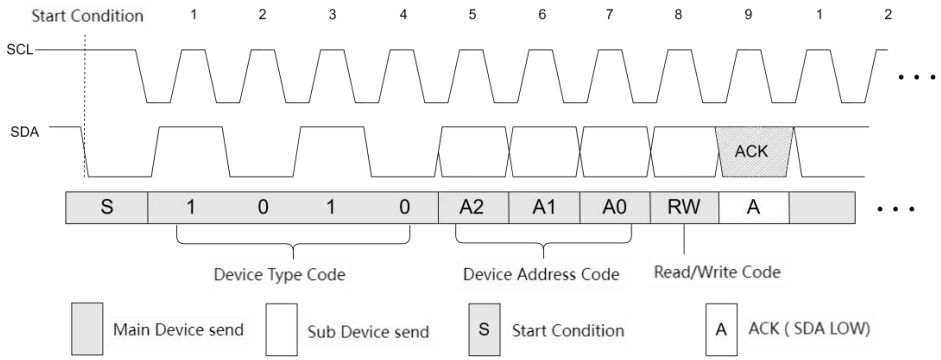


Figure 5：Device address word timing diagram

3.3 Write Operation

All write operations, including the single-byte write shown in Figure 6 and the multi-byte write shown in Figure 7, first send the start condition, then send the device address word, and then send the memory address to be accessed and the data to be written.

The R/W bit of bit0 in the device address word should be set to 0 to indicate a write operation: the slave will generate an acknowledgement signal (ACK) after successfully receiving 8 bits of data from the host, and a non-acknowledgement signal (NACK) if the reception fails; the host can write any number of bytes as needed in a write operation, and after receiving the slave's acknowledgement signal, the write operation ends with a stop condition (P): the data will be written to the memory in ascending order with the input memory address as the starting address, and the address counter will roll back to 0000h after reaching the 7FFFh.

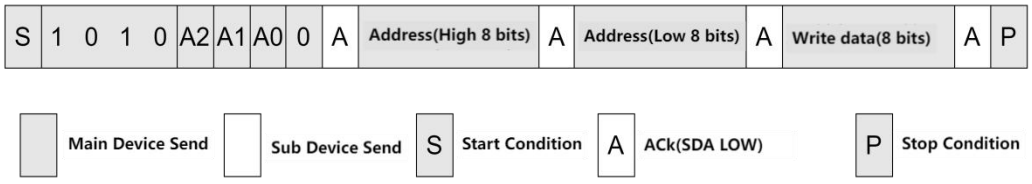


Figure 6：Single byte write diagram

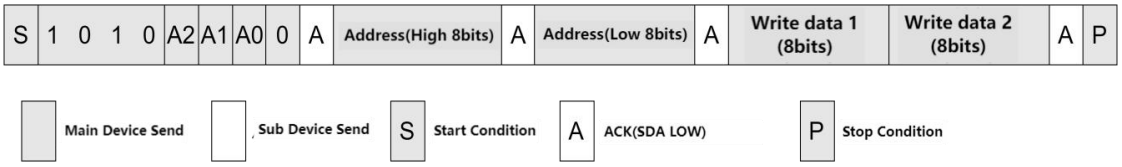


Figure 7：Schematic diagram of multi-byte writing (taking two bytes as an example)

Unlike other non-volatile storage technologies, MRAM has no write delay. This is because the write and read cycles of the storage array are almost equal and are very short compared to the bus clock. For users, both write and read operations can be initiated immediately after the last write operation is completed, without a certain delay, and without the need for polling confirmation after the write operation like EEPROM chips. If polling confirmation is performed, the result is often that the write is completed and subsequent operations can be performed.

3.4 Read operation

Read operation can be divided into three types: current address read, random address read and sequential read.

Current address read

After a write or read operation is successfully completed and ends normally with a stop condition, assuming that the last accessed address is n, if the power is not turned off during the period, the data of address n+1 can be read by sending the following command. If n is the last address 7FFFh, then n+1 will point to address 0000h; if the power is turned off during the period and then turned on again, the current address n will become undefined.

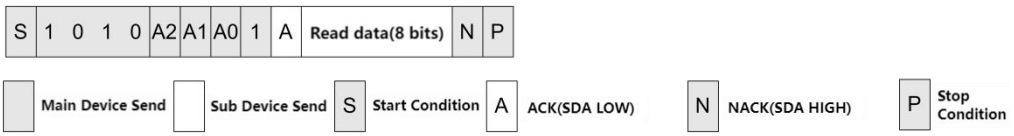


Figure 8 Current address read

Random address read

Random address read provides users with a simple operation to read any address, as shown in the figure below. The instruction can be divided into two parts:

1. The first three bytes are the same as the write operation, and the R/W bit must be set to 0 to set the memory address to be accessed.

2. The latter part starting from the second S is the same as the current address read operation, and the R/W bit must be set to 1 to read the data in the specified address.

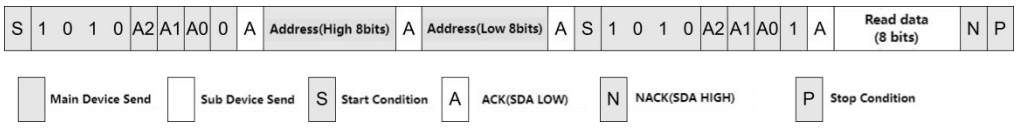


Figure 9 Random address read

Sequential Read

By specifying the address in the same way as random read, data can be received continuously after the device address word (input R/W "1"). If the read exceeds the end of the address by 7FFFh, the read address automatically rolls back to 0000h and continues reading.

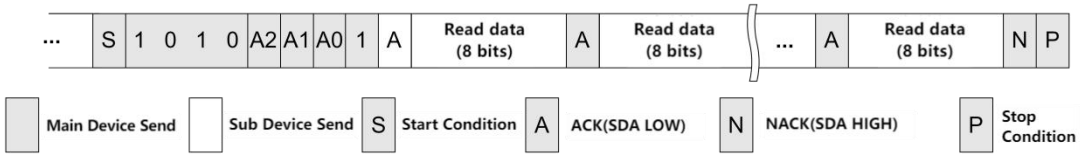


Figure 10 Sequential Read

3.5 Sleep Mode

Sleep mode is a low power mode that is entered and exited by the following instructions.

Entering Sleep Mode

The operation of entering sleep mode is as follows:

1. The host sends a start condition (S);

2. The host sends the command F8h;

3. The slave sends ACK;

4. The host sends an 8-bit device address word, where the R/W bit (bit0) can be sent as 0 or 1;

5. The slave sends ACK.

6. The host sends a start condition (S) again;

7. The host sends the command 86h;

8. The slave sends ACK;

9. The host sends STOP to ensure that the device enters sleep mode.

Figure 11 Enter sleep mode

Exit sleep mode command

In sleep mode, the chip also detects the status of the SDA and SCL pins in real time. When the exit sleep mode command is received and the t_{REC} wake-up time is reached, the chip exits sleep mode.

The operation of exiting sleep mode is as follows:

1. The host sends the start condition (S), followed by an 8-bit device address word, where the R/W bit (bit0) can send either 0 or 1:

2. At the rising edge of the 9th clock starting from the start condition, the recovery operation begins, turning on the internal power supply one by one:

3. After the wake-up time (t_{REC}), the power supply is stable, the chip exits sleep mode, returns to the standby state, and can be read and written.

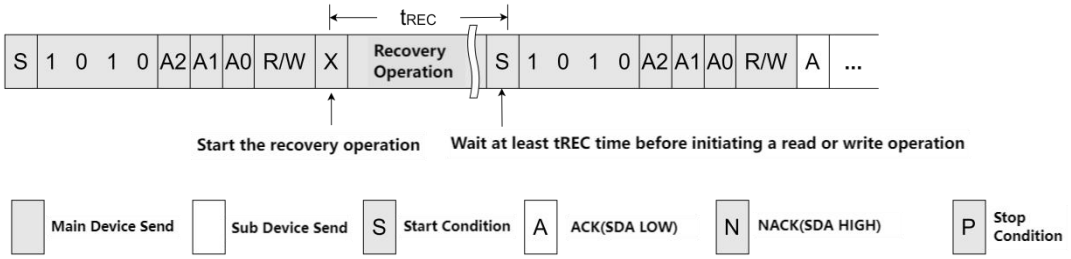


Figure 12 Exit sleep mode

3.6 Device ID

Device ID consists of 3 bytes, which is read-only information and includes Manufacturer ID and Product ID. The bit distribution information is shown in the following table.

Table 2 Device ID Bit Table

Device ID	
23-12 (12 bits)	11-0(12 bits)
Manufacturer ID	Product ID

Device ID can be accessed in the following ways:

1. The host sends a start condition (S);

2. The host sends the command F8h;

3. The slave sends ACK;

4. The host sends an 8-bit device address word, where the R/W bit (bit0) can be 0 or 1;

5. The slave sends ACK:

6. The host sends a start condition (S) again;

7. The host sends the command F9h;

8. The slave sends ACK;

9. The host receives the Device ID byte and sends ACK to indicate that it continues to receive until the last byte is received. It ends the Device ID read operation by sending NACK:

10. The host sends a stop condition (P) to end this operation, and the slave device returns to the standby state.

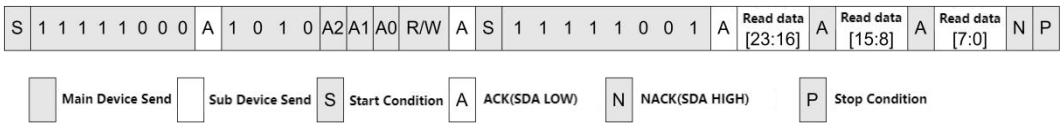


Figure 13 Read DEVICE

3.7 Serial Number

Serial numbers consist of eight bytes and are read-only information that can be used to uniquely identify a pc board or system.

Serial Number similar to reading Device ID. The specific operations are as follows:

1. The host sends a start condition (S);

2. The host sends the command F8h;

3. The slave sends ACK:

4. The host sends an 8-bit device address word, where the R/W bit (bit0) can send 0 or 1;

5. The slave sends ACK;

6. The host sends a start condition (S) again;

7. The host sends the command CDh to read the Serial Number.

8. The slave sends ACK;

9. The host receives the Serial Number byte and sends ACK to indicate that it continues to receive until the last byte is received. The host ends the Serial Number reading operation by sending NACK;

10. The host sends a stop condition (P) to end this operation, and the slave device returns to the standby state.

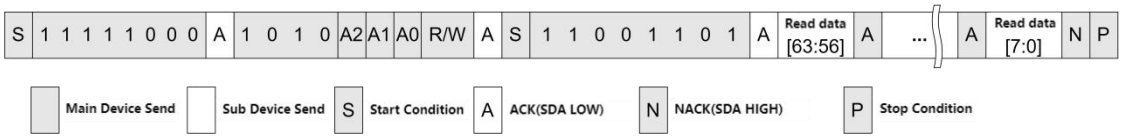


Figure 14 Read Serial Number

4 Absolute Maximum Rating

Table 3:Absolute Maximum Rating

Symbol	Parameter	Test Conditions	Value	Unit
VCC	Voltage Supply		0 to 3.6	V
Vin	Voltage on any pin		0 to 3.6	V
Iout	Output current per pin		±3	mA
Tbias	Temperature under bias		-40 to 85	℃
Tstg	Storage Temperature		-55 to 125	℃
Tlead	Lead temperature during solder(3mins max)		260	℃
Hmax write	Maximum magnetic field during write*1	Write	4,000	A/m
Hmax read	Maximum magnetic field during read or standby*1	Read or Standby	12,000	A/m
Hmax power off	Maximum magnetic field during power off*1	Power off	45,000	A/m

Note:

The test conditions are room temperature and exposure to vertical magnetic field for one month to measure the anti-magnetic ability.

5 Electrical Characteristics

This chapter introduces the electrical characteristics of the chip. The AC and DC parameter values shown in the following table are obtained based on the operating conditions shown in Table 4 and the measurement conditions marked in Table 5. When users check a parameter, pay attention to matching the operating conditions and measurement conditions.

5.1 Operating Conditions

Table 4 Operating Conditions

Symbol	Parameter	Min	Max	Unit
VCC	Voltage Supply	2.7	3.6	V
Tax	Operating Temperature	-40	85	℃

5.2 DC characteristic

Table 5 DC characteristic

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$\|I_{LI}\|$	Input leakage current *1	V_{IN}=0V~VCC			1	μA
$\|I_{LO}\|$	Output Leakage current*2	V_{OUT}=0 V~VCC			1	μA
I_{SLP}	Sleep Current	SCL、SDA=VCC, A0、A1、A2、WP=0V		2	6	μA
I_{SBY}	Standby current	SCL、SDA= VCC , AO、A1、A2、WP =0Vor VCC or floating*3		20	35	μA
I_{CC}	Active Current	SCL=400KHz		400	600	μA
V_{IL}	Input low voltage	VCC=2.7V~3.6V	VSS		VCC*0.2	V
V_{IH}	Input high voltage	VCC=2.7V~3.6V	VCC*0.8		VCC+0.3	V
V_{OL}	Output low voltage	I_{OL}=3mA			VCC*0.2	V
R_{IN}	Input resistance(WP、A0、A1、A2)	V_{IN}=V_{IL}(Max)	50			kΩ
		V_{IN}= V_{IH}(Min)	1			MΩ

Notes:

1. Applicable to SCL and SDA pins.
2. Applicable to SDA pin.
3. In addition to the pin level status in the table, the sleep mode test conditions must also ensure that the measurement time is after the stop condition, and cannot be measured when the instruction is halfway sent.

5.3 Pin capacitance

Table 6 Pin capacitance

Symbol	Parameter	Max	Unit
C_{IN}	Control input capacitance	15	pF
C_{IO}	IO capacitance	15	pF

5.4 AC Features

Table 7 AC Features

Symbol	Parameter	100kHz		400kHz		Unit
		Min	Max	Min	Max	
t_{CLK}	CLK period	10		2.5		μs
t_{HIGH}	Clock high	4		0.6		μs
t_{LOW}	Clock low	4.7		1.3		μs
t_R	SCL, SDA rise time		1000		300	ns
t_F	SCL, SDA fall time		300		300	ns
$t_{HD:STA}$	Hold time of start condition	4		0.6		μs
$t_{SU:STA}$	Start condition setup time	4.7		0.6		μs
$t_{HD:DAT}$	Data input hold time	2		2		ns
$t_{SU:DAT}$	Data input setup time	250		100		ns
$t_{DH:DAT}$	Data output hold time	0		0		ns
$t_{SU:STO}$	Stop condition setup time	4		0.6		μs
t_{AA}	SCL low level to output data valid		3		0.9	μs
t_{BUF}	Precharge time (interval between stop condition and start condition)	4.7		1.3		μs

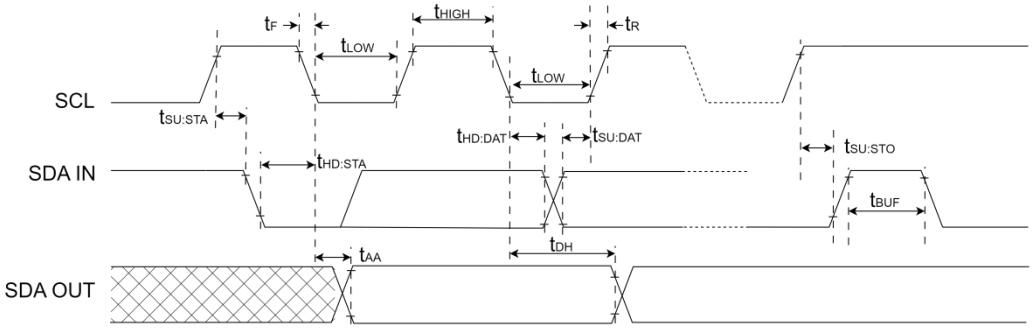


Figure 15 AC Timing Definition

5.5 Power-on/Power-off Characteristics

In order to protect data during power-on, the chip does not support read or write operations when VCC is lower than VCC(min); VCC(min) refers to the minimum VCC value specified when the chip is working normally, which is 2.7V in this chip, and VCC(max) refers to the maximum VCC value specified when the chip is working normally, which is 3.6V in this chip.

During the power-on, you must wait for t_{PU} time (power-on delay time) after the voltage rises to VCC(min) before the chip can start working normally. This time is used to ensure that the internal voltage of the chip has stabilized. t_{PU} is measured from the time VCC reaches VCC(min).

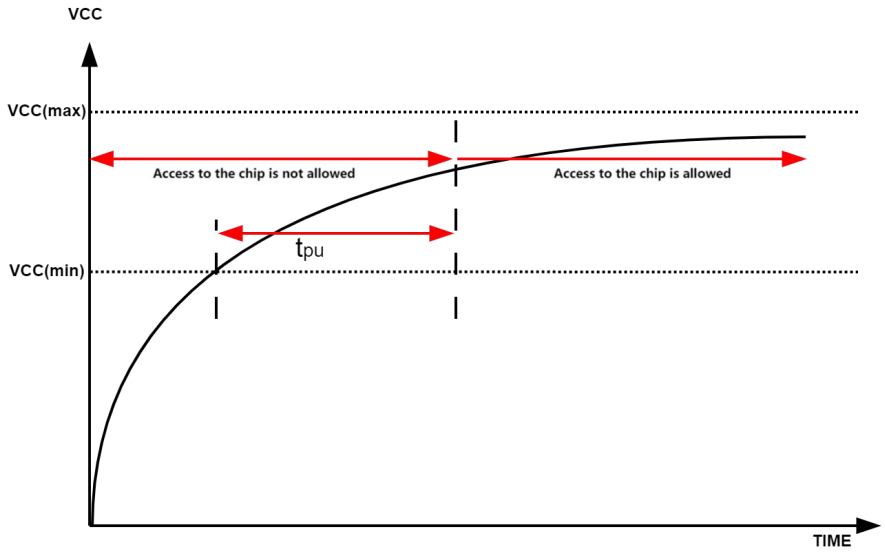


Figure 16 Power-on process diagram

At power-on, in order to properly initialize the chip, the following steps need to be performed:

(1) Increase VCC (after t_{RVR} time);

(2) When VCC is lower than VCC(min), it is recommended not to send instructions to the chip;

(3) During the initial power-on period or after power-off and power-on, it is necessary to wait for t_{PU} before accessing;

(4) After power-on, the chip is in standby mode.

When the chip is powered off or out of power, please follow the following steps to properly shut down the device:

(1) Reduce VCC to below VCC_RST;

(2) When VCC is lower than VCC(min), it is not allowed to send instructions to the chip;

(3) After power-off, when VCC rises to above VCC(min), it is necessary to follow the power-on initialization process;

(4) In order to stabilize the VCC level, it is recommended to add a suitable decoupling capacitor to the VCC pin;

(5) If VCC rises from a voltage between VCC_ RST and VCC(min) to VCC, the chip is not guaranteed to work properly.

Table 8 Chip power-on/power-off parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{PU}	Power Up delay time	100	-	-	μs
t_{RVR}	Rise time from VCC to VCC(min)	-	-	30	ms
t_{RVF}	Falling time from VCC to VCC_RST	20	-		μs
VCC_RST	VCC reset voltage	0	-	2	V
t_{PLOW}	VCC low level time	50	-	-	ms
t_{REC}	Sleep wake-up time	16	-	-	us

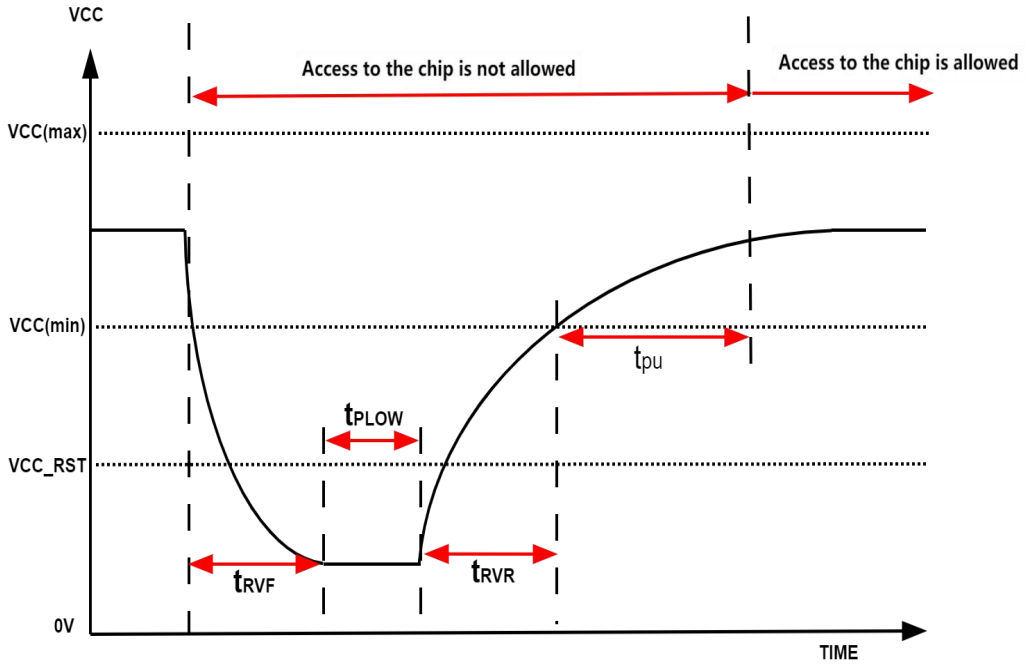
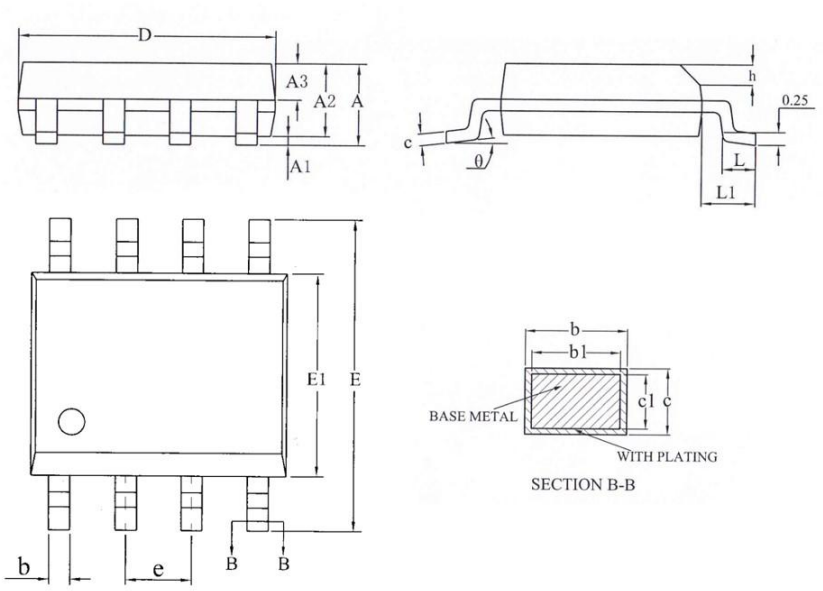


Figure 17 Power-off and power-on process diagram

6 Usage Notes

We recommend users to program the chip after reflow, because we cannot guarantee that the data written before reflow will still be valid after reflow.

7 Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 18: SOP8 Package Outline

Special Instructions

The company reserves the right of final interpretation of this specification

Version Change Description

Version: V1.0 Author: Zhao Time: 2025.03

Modify the record：

1. First Edition

Statement

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